EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 01128297
PUBLICATION DATE : 19-05-89

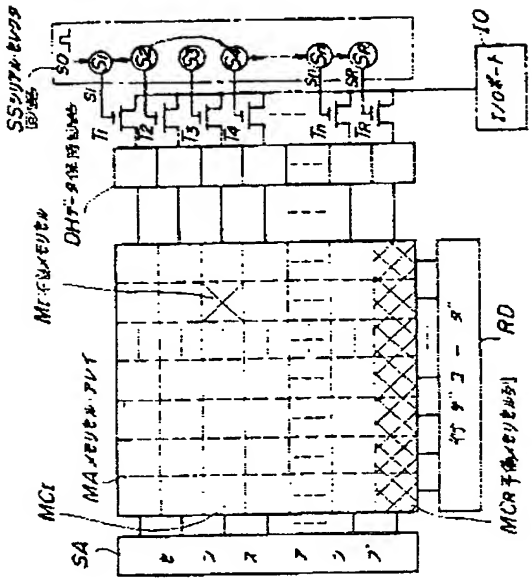
APPLICATION DATE : 12-11-87
APPLICATION NUMBER : 62286705

APPLICANT : SHARP CORP;

INVENTOR : MATSUURA YOSHIAKI;

INT.CL. : G11C 29/00 G11C 11/34

TITLE : SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



ABSTRACT : PURPOSE: To reduce a defective generating rate by constituting the selected circuit with the switching of a defective selected circuit to a normal selected circuit when the defective selected circuit exists in the plural selected circuits.

CONSTITUTION: When a defective memory MI exists at a position shown in a figure, the fuse link of a selector S_3 corresponding to a memory cell array MCI to which the defective memory cell belongs is disconnected. Further, the fuse link of a spare selector SR is disconnected. Thus, the selective signal is outputted as $S_1 \rightarrow S_2 \rightarrow S_4 \rightarrow SR$, the memory cell array MCI to which the defective memory cell MI belongs is jumped off, and a spare memory cell array MCR is selected instead of it. Thus, the defective generating rate can be reduced.